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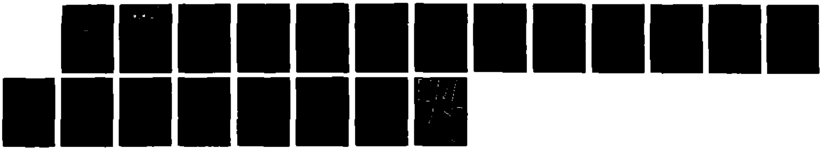

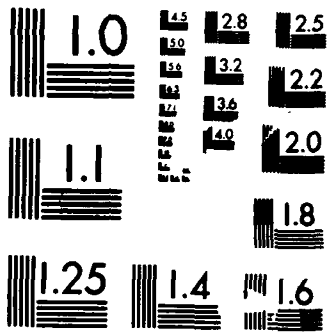

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FAULT-TOLERANT MULTIPROCESSOR AND VLSI-BASED SYSTEMS

Interim Report for AFOSR 84-0052

Period covered: January 1985 through January 1986

Principal Investigator: Dhiraj K. Pradhan

Department of Electrical and Computer Engineering

University of Massachusetts

Amherst, Massachusetts

Abstract

This report summarizes research performed under the auspices of AFOSR84-0052 during the period of January 1985 through January 1986. Also included is a list of publications, along with copies of papers published during this period. The indicated future directions of this research are outlined, as well.

INTRODUCTION

An overview is provided in this report of the various research that has been carried out during the period of January 1985 through January 1986, under the sponsorship of the grant AFOSR 84-0052. Organized into three main sections, Section II reviews the different forms that the on-going research has taken, and highlights some of the key results. Section III then goes on to list all of the publications that have directly resulted from this grant during this timeframe, and delineates the names of those students supported. Section IV looks carefully into future directions indicated for the on-going research. The report concludes with a copy of each publication previously mentioned in Section III, coupled with the principal investigator's vita.

Research has primarily focused, this past year, on the following topics:

1.1 Modelling the effect of redundancy on both the yield as well as the performance of VLSI systems.

1.2 Developing a framework for wafer-scale integration of multiprocessor systems.

1.3 Developing a DeBruijn multiprocessor network as a versatile parallel processing network, suitable for VLSI.

1.4 Conceptually formulating a fault-tolerant architecture for large RAMs.

The following section further elaborates on these research results.

II. SUMMARY OF RESEARCH RESULTS

This section is organized into four main parts which correspond to the four different topics outlined in Section I.

2.1 Incorporating different forms of redundancy has recently been proposed for various VLSI and WSI designs. These include regular architectures, built by interconnecting a large number of few types of system elements on a single chip or wafer. The motivation for introducing fault tolerance (redundancy) into these architectures is two-fold; yield enhancement and performance improvement.

VLSI and WSI architectures that use redundancy for yield and performance improvement are precisely what have been considered here. The available redundancy on the chip or wafer is limited primarily by the size of the chip or wafer; hence, to find a method by which one can optimally share the available redundancy between yield enhancement and performance improvement is imperative.

What we have developed are analytical models for the evaluation of performance and yield improvement through redundancy. For these two somewhat competing requirements, our proposed models can be effectively used to study the effect of sharing element level and system level redundancy. One very significant aspect about this research is that no such models have been available earlier. In fact, to the best of our knowledge, ours is the first attempt to model these complex interrelationships.

Certain preliminary results were already presented and well received at the Fifteenth International Symposium on Fault-Tolerant Computing, held in June 1985. The more complete and fully developed work in the subject has since been submitted for publication, to IEEE Transactions on Computers.

2.2 Wafer-Scale integration provides several important advantages to the design of complete systems on one piece of silicon - advantages like faster communications, fewer packaging steps and less stringent pin limitation. New problems, though, accompany "WSI", which do not exist when the different elements of a system are implemented on separate silicon chips. Defective system elements, for instance, can neither be repaired nor discarded; they must be dealt with by introducing fault-tolerance into the architecture of the designed system, itself. Also, all designed elements must share the same silicon area and the same allowed power dissipation. Consequently, it must be determined how best to partition the available area and the total allowed power dissipation among the different types of elements, so as to optimize cost function. Such design problems can very well lead to changes in well-established system architectures as well as development of new ones which may be more appropriate to wafer-scale integration.

What our research develops is a new design environment, via the examples of closely-coupled multi-processor systems. We have also formulated several cost functions, to optimize in this environment.

2.3 The binary de Bruijn multiprocessor network (BDM) has been seriously investigated, to determine how it can solve a wide variety of classes of problems. For instance, it has been observed that the BDM admits an N-node linear array, an N-node ring, (N-1)-node complete binary trees, ((3N/4-2)-node tree machines and an N-node one-step shuffle-exchange network (where N ($=2^k$, k is an integer) is the total number of nodes). In particular, a $\Theta(N)$-time algorithm is provided which is able to find a linear array between the nodes 0 and N-1 in the BDM.

The de Bruijn multiprocessor networks are also shown to be fault-tolerant, as well as being extensible. A tight lower bound of the VLSI layout area of the BDM has been derived; a procedure for an area-optimal VLSI layout also has been produced. Finally, we were able to demonstrate, too, that the BDM is more versatile that the shuffle-exchange (SE) and the cube connected cycles (CCC).

2.4 Soon, dynamic RAMs will reach the multi-megabit range. Our work proposes a new architecture for these devices, able to solve some of the problems associated with the 'four quadrant' architecture. Applying the principle of divide and conquer, the RAM is partitioned into modules, each appearing as the leaf node of a binary interconnect network. This network carries the address/data/control bus, permitting the nodes to communicate between themselves and the outside world. This architecture is shown to be fault tolerant, improving both yield and reliability. Also, it is easily partitionable, improving the probability of generating partially good products. Parallelism in testing, and partial self test in these RAMs results in a dramatic savings of testing time. Finally, unlike other fault tolerant/testability schemes, this approach promises improved performance, in terms of lower access times as well as reduction in the time required to refresh the device. These benefits are obtained at only a small increase in chip area. Also developed are detailed area/time cost analyses, test algorithms and some preliminary implementation results. The preliminary results on this work have been recently submitted for publication.

Finally, in addition to the above-reported results, we have developed some key results in the area of system level diagnosis of multiprocessor

systems. What we have come up with is a new approach that dynamically adapts the testing to the actual number of faults in hand. This has the added advantage of being able to greatly benefit reducing the testing complexity, as faults are expected to occur progressively.

III. PUBLICATION AND STUDENT SUPPORTED

1. Pradhan, D.K., "Fault-Tolerant Multilink Multibus Structures," IEEE Transactions on Computers, Vol. C-34, No. 1, pp. 34-45, January 1985.

2. Pradhan, D.K., "Dynamically Restructurable Fault-Tolerant Processor Network Architectures," IEEE Transactions on Computers, Vol. C-34, No. 5, pp. 434-447, May 1985.

3. Koren, I. and D.K. Pradhan, "Introducing Redundancy into VLSI Designs for Yield and Performance Enhancement," Proc. FTCS-15, pp. 330-334, Ann Arbor, Michigan, June 1985.

4. Meyer, F.J. and D.K. Pradhan, "Dynamic Testing Strategy for Distributed Systems," Proc. FTCS-15, pp. 84-90, Ann Arbor, Michigan, June 1985.

5. Samatham, M. and D.K. Pradhan, "A Versatile Sorting Network," Proc. 12th ACM/IEEE Annual Symposium on Computer Architecture, pp. 360-367, Boston, Massachusetts, June 1985.

Research Assistants Supported by AFOSR

Fred J. Meyer (1st year Ph.D. student)

M.R. Samatham (2nd year Ph.D. student)

IV. FUTURE DIRECTION OF RESEARCH

Our plans incorporate the need to continue research on the various topics outlined in Section II with a concentration of efforts on developing a design environment for a multi-processor system on a single large area chip, while exploring the testable and fault-tolerant RAM design developed here. We are particularly excited about this RAM design as it has received enthusiastic reviews from industrial and academic sources, alike.

A multi-processor system implemented on a single silicon chip can benefit from the primary advantages of wafer-scale integration - faster communications among the various system elements, less expensive manufacturing steps (i.e., eliminating the need to dice the wafer into individual chips as well as having bond to their pads to external pins). Additionally, by implementing the entire system on one piece of silicon, all previously external interconnections are turned into internal ones, avoiding in this way the problem of pin limitation.

The well-established architectures of closely-coupled multi-processor systems, though, are not always suitable for direct VLSI implementation. Primarily, this is due to the fact that different constraints have to be dealt with, in this new design environment. First, there is a finite amount of silicon area which all types of system elements must share; this is a constraint that does not exist when every system element is manufactured on a separate silicon chip. What this implies is that we have to determine how many elements of each type (e.g., processors, memory modules, etc.) should we include in our design, given the area required by each of these elements. This has to be determined in such a way so that some system cost function (e.g., some performance measure) will be optimized.

Secondly, the fact that all of the elements of the multi-processor system share the same piece of silicon poses a restriction on the total amount of power that can be dissipated by the system. In most cases, this restriction is more severe that the equivalent one for ordinary multi-processors. If not all system elements dissipate the same amount of power, the above restriction may result in the inclusion of less than the optimal number of the high-power elements.

Thirdly, in the traditional assembling of multi-processors, only defect-free ICs are used while the defective ones are discarded. There are two important implications here: redundancy must be incorporated into the design so that we will be able to use the system in the presence of defects and that, the system has to be designed in such a way that will allow us to interconnect most (if not all) of the defect-free elements so as to form an operational multiprocessor. Thus, fault-tolerant architectures must be devised for these multi-processor systems so that they can be implemented on one piece of silicon.

These three factors, the finite amount of silicon area, the limited power dissipation and the need for fault-tolerance, may lead to different optimal designs of existing architectures, as well as to the development of new architecture. What we are here developing are various analytical tools which will facilitate the realization of multiprocessor systems on a single VLSI chip.

The other desired thrust for the future will be directed toward the area of testable fault-tolerant RAM design. Advances in RAM design over the past decade have been reflected in the amount of memory available on a chip. Quadrupaling every 2 or 3 years, from 1K to 4K, 16K, 64K and 256K, 1M RAMs

soon will be available; coupled with the advances in WSI densities of M and 16M, they may soon be practical, too.

Several reasons are behind this development. The first reflects the evolution of the storage cell in a RAM. From the initial 6 transistor static cell, it has evolved to the 1 transistor dynamic cell. The subject of considerable research, this cell has seen a large number of variations proposed. These designs have varying features such as higher charge storage capability, lower leakage, immunity to alpha particle radiation, etc. The saving in area due to this cell has made possible larger amount of memory on a chip.

A second reason underlying development is the improvement in fabrication technology, causing the feature size to progressively shrink from 6μm in 1978 to 1.5μm today. Devices with submicron feature sizes have been successfully fabricated in laboratories. Since reducing the feature size by a factor of 2 results in quadrupaling the amount of circuitry for a given area, this development has been responsible for not only increasing the amount of memory on a chip, but for major advances in VLSI.

Finally, use of redundant word and bit lines to correct faults in either the cell array or the decoder has made possible the development of 64K and larger RAMs. Use of on chip error correcting codes has also been explored. This, together with a better understanding of the failure mechanisms and development of good yield models have, to a real extent, overcome the yield problems that these devices faced.

Our plan is to pursue a new concept in RAM design developed thus far. This design is novel in that it combines both the features of testability and fault-tolerance. What is even more important is that our design

achieves even better performance than the conventional RAM design. This improvement in performance is realized by trading off interconnections within the storage subarray with division of the array into smaller subarrays.

Also what is important to note is that through this RAM design, we have been able to develop a new concept in VLSI design which allows both testability and fault-tolerance to be incorporated through shared redundancy. This concept needs to be further developed as a general theory in digital system design.

APPENDIX

Vita of Principal Investigator

Copies of Publications

Biography

Dhiraj K. Pradhan

Dr. Dhiraj K. Pradhan is currently a Professor in the Department of Electrical and Computer Engineering, University of Massachusetts, Amherst. Previously, he has held positions with the University of Regina, Sask. Canada, Oakland University, Rochester, MI, Stanford University, Stanford, CA, and IBM Corporation. He has been actively involved with research in fault- tolerant computing and parallel processing since receiving his Ph.D. in 1972. He has presented numerous papers on fault-tolerant computing and parallel processing. He has also published extensively in journals such as *IEEE Transactions* and *Networks*. His research interests include fault- tolerant computing, computer architecture, graph theory, and flow networks.

Dr. Pradhan has edited the special issue on Fault-Tolerant Computing, published in *IEEE Transactions on Computers* (April 1986) and *IEEE Computer*, (March 1980). Also he has served as Session Chairman and Program Committee Member for various conferences. Currently he is an Editor for the *Journal of VLSI and Digital Systems*. He is also the editor and coauthor of the book entitled, *Fault-Tolerant Computing: Theory and Techniques*, Vol. I and II, published by Prentice-Hall.

Dhiraj K. Pradhan

CURRICULUM VITAE

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Positions–Academic

1/83 – present	Professor; Department of Electrical and Computer Engineering, University of Massachusetts, Amherst, Massachusetts.
6/79 – 8/79	Research Associate Professor; Stanford University; Computer Systems Lab.; Stanford, California.
9/78 – 12/82	Associate Professor; School of Engineering, Oakland University, Rochester, Michigan.
6/82 – 8/82	Visiting Research Professor; Department of Electrical Engineering and Computer Science; University of California; Berkeley, California.
9/73 – 7/78	Associate Professor; Department of Computer Science; University of Regina; Regina, Canada. (9/73–7/76, Assistant Professor).

Positions–Industrial

10/72 – 8/73	Staff Engineer; (fault-tolerant group); IBM; Systems Development Lab.; Poughkeepsie, New York.
1982 – present	Consultant to Mitre GTE and CDC in fault-tolerant computing.

Education

1972, Ph.D.	(Electrical Engineering); University of Iowa; Iowa City, Iowa. Thesis area: Fault-Tolerant Computing
1970, M.S.	(Electrical Engineering); Brown University; Providence, Rhode Island. Thesis area: Complexity Theory

Personal

Born on December 1, 1948, Married, Three Children, U.S. Citizen

Professional Activities *(Highlights)*

1985 – 1986	Guest Editor, IEEE Transactions on Computers, Special Issue on Fault-Tolerant Computing, April, 1986.
1982 – 1985	IEEE Distinguished Visitor, Computer Society

1983 – 1984	Member, Program Committee, 11th Annual International Symposium on Computer Architecture.
1981 –	Editor, Journal of VLSI and Digital Systems, Computer Science Press, Maryland.
1980 – 1981	Member, Program Committee, International Symposium on Fault-Tolerant Computing, June 81.
1979 – 1980	Guest Editor; Special Issue on Fault-Tolerant Computing; IEEE Computer, March 1980.
1980 – 1986	Session Chairman, ACM/IEEE Joint Computer Conference, ICCD, Compcon, International Symposium on Fault-Tolerant Computing, International Symposium on Multivalued Logic, Evanston, Illinois.
1980	Invited Paper, Fault–Tolerant VLSI Workshop, Los Angeles, California, Multivalued Logic Conference
1975 – 1984	Invited Lecturer; Cesellschaft fur Mathematik und Datenverarbeitung; mbh Bonn; Bonn, West Germany, National Defense Academy, Yokosuka, Japan and others.

Research Supervision

1978 – present	Several Ph.D. and M.S. Students.
1982 – 1985	Two Post-doctoral fellows.
1977 – 1978	One Post-doctoral fellow.
1975 – 1977	One Post–doctoral fellow.

Research Grants

1973 – present	PI to Multiple grants from NSF, AFOSR and NRC (Canada)

List of Publications

Text Book

Fault-tolerant Computing: Theory and Techniques, Vol. I and Vol. II, Prentice-Hall, Inc., May 1986. (Editor and Co–Author).

In Journals:

1. "Modelling the Effect of Redundancy on Yield and Performance of VLSI Systems," IEEE Transaction on Computers, 1987 (in press).
2. "Yield and Performance Enhancement through Redundancy in VLSI and WSI Multiprocessor Systems," Proceeding of IEEE, (with I. Koren) May 1986.
3. "Introducing Redundancy into VLSI Designs for Yield and Performance Enhancement," Proc. FTCS-15, Ann Arbor, Michigan (with Israel Koren).
4. "Dynamically Restructurable Fault-tolerant Processor Network Architectures," IEEE

Transactions on Computers, May 1985.

5. "Fault-tolerant Multilink Multibus Structures," IEEE Transactions on Computers, Vol. C-34, No. 1, January 1985.
6. "Synthesis of Directed Multi-Commodity Flow Problems," Networks, (with A. Itai) Vol. 14, 1984, pp. 213-224.
7. "Sequential Network Design Using Extra Inputs for Fault Detection," IEEE Transactions on Computers, Vol. C-32, No.3, March, 1983.
8. "A Fault-Tolerant Distributed Processor Communication Architecture," IEEE Transactions on Computers, September, 1982, pp. 863-870 (with S. Reddy).
9. "A Class of Unidirectional Error Correcting Codes," IEEE Transactions on Computers, June, 1982, pp. 564-568 (with B. Bose).
10. "A Uniform Representation of Permutation Networks Used in Memory- Processor Interconnection," IEEE Transactions on Computers, Special Issues on Parallel Processing, September, 1980, (with K.L. Kodandapani), pp. 777-791.
11. "A New Class of Error Correcting-Detecting Codes for Fault-Tolerant Computer Applications," IEEE Transactions on Computers, Vol. C-29, No. 6, pp. 471-481, June, 1980.
12. "Error-Correcting Codes and Self-Checking Circuits," IEEE Computer, Vol. 13, Number 3, pp. 27-38, March, 1980 (with J.J. Stiffler).
13. "Undetectability of Bridging Faults and Vaildity of Stuck-at Fault Test Sets," IEEE Transactions on Computers, Vol. C-29, No. 1, (with K.L. Kodandapani) p. 55-59, January, 1980.
14. "Fault-Tolerant Asynchronous Networks Using Read-Only Memories," IEEE Transactions on Computers, Vol. C-27, No. 7, pp. 674-679, July 1978.
15. "Fault Secure Asynchronous Networks," IEEE Transactions on Computers, Vol. C-27, No. 5, pp. 396-404, May 1978.
16. "A Theory of Galois Switching Functions," IEEE Transactions on Computer, Vol. C-27, No. 3, pp. 239-249, March 1978.
17. "Universal Test Sets for Multiple Fault Detection in AND-EXOR Arrays, " IEEE Transaction on Computers, Vol. C-27, No. 2, pp. 181-187, February 1978.
18. "Store Address Generator with Built-In Fault Detection Capabilities," IEEE Transactions on Computers, Vol. C-26, No. 11, pp. 1144-1147, November 1977, (with M.Y. Hsiao & A.M. Patel).
19. "A Graph-Structural Approach for the Generalization of Data Management Systems," Information Sciences, American Elesevier Publishing Company, Inc., pp. 1-17, March 1977.
20. "Techniques to Construct (2,1) Seperating Systems from Linear Codes," IEEE Transactions on Computers, (with S.M. Reddy), Vol. C-25, No. 9, pp. 945-949, September 1976.
21. "Reed-Muller Canonic Forms for Multivalued Functions," IEEE Transactions on Computers, (with A.M. Patel), Vol. C-24, No. 2, pp. 206- 220, February 1975.
22. "Fault-Tolerant Carry Save Adders," IEEE Transactions on Computers, Vol. C-23, No. 11, pp. 1320-1322.
23. "Design of Two-Level Fault-Tolerant Networks," IEEE Transactions on Computers, Vol. C-23, No. 1, pp. 41-48, (with S.M. Reddy), June 1974.
24. "Fault-Tolerant Asynchronous Networks," IEEE Transactions on Computers, Vol. C-22, No. 7, pp. 662-669, (with S.M. Reddy), July 1973.

In Conference Proceedings

25. "Introducing Redundancy into VLSI Designs for Yield and Performance Enhancement," Proc. FTCS-15, pp. 330-334, Ann Arbor, Michigan (with Israel Koren), June 1985.
26. "Dynamic Testing Strategy for Distributed Systems," Proc. FTCS-15, Ann Arbor, Michigan, (with Fred Meyer), June 1985.
27. "A Versatile Sorting Network," Proc. 12th Annual Symposium on Computer Architecture, (with M.R. Samatham), June 1985.
28. "Fault-tolerant Multibus Architectures for Multiprocessors," Proc. FTCS-14, June 1984, Kissime, Florida, (with M.L. Schlumberger and Z. Hanquan) pp. 400-408.
29. "A Multiprocessor Network Suitable for Single Chip VLSI Implementation," Proc. 1984 IEEE 11th Annual Int. Symp. on Computer Architecture, June 1984, pp. 328-337.
30. "Fault-Tolerant Network Architectures for Multiprocessors and VLSI Based Systems," Proc. FTCS-13, Milan, Italy, June, 1983.
31. "On a Class of Multiprocessor Network Architectures," Proc. of International Conference on Distributed Processing, Miami, Florida, October, 1982, pp. 302-311, (Also reprinted in Interconnection Networks for Parallel and Distributed Processing edited by C. Wu and T. Feng, Aug. 1984).
32. "Interconnections Topologies for Fault-Tolerant Parallel and Distributed Architectures," Proc. of 10th International Conference on Parallel Processing, pp. 238-242, August, 1981.
33. "Testing for Delay Faults in a PLA," Proc. International Conference on Circuits and Computers, (with K. Son) September 1982, pp. 346-349.
34. "Fault-Diagnosis of Parallel Processor Interconnection Networks," Proc. Eleventh Annual International Symposium on Fault-Tolerant Computing, pp. 209-212, June, 1981 (with K.M. Falavarajani).
35. "A Fault-Tolerant Communication Architecture for Distributed Systems," Proc. Eleventh International Conference on Parallel Processing, pp. 214-220, June, 1981.
36. "A Solution to Load-Balancing and Fault Recovery in Distributed Systems," Symposium on Reliability in Distributed Software and Database Systems, July, 1981, pp. 89-94.
37. "A Fault-Diagnosis Technique for Closed Flow Networks," Proc. of 1980 Symposium on Fault-Tolerant Computing, Kyoto, Japan, October 1980.
38. "Completely Self-Checking Checkers," Digest of 1981 Test Conf., (with K. Son), pp. 231-237, October 1981.
39. "Effect of Undetectable Faults on Testing PLAs," Digest of 1980 Test Conf., (with K. Son), November 1980.
40. "An Easily Testable Design of PLAs," Cherry Hill Test Conference, Philidelphia, Pennsylvania, (with K. Son), November 1980. (Reprinted in IEEE Tutorial on VLSI Testing by Rex Rice).
41. "A Generalization of Shuffle-Exchange Networks," Proc. of Fouteenth Annual Conference on Information Sciences and Systems, Princeton, New Jersey, March 1980.
42. "A Framework for the Study of Permutations and Applications to Memory Processor Interconnection Networks," Proc. 1979 International Conference on Parallel Processing, (with K.L. Kodandapani), pp. 148-158, August 1979.

43. "Shift Registers Designed for On-Line Fault Detection," Proc. of 1978 International Symposium on Fault Tolerant Computing, Toulous, France, pp. 173-178, June 1978.

44. "A Synthesis Algorithm of Directed Two-Commodity Networks," 1978 IEEE International Symposium on Circuits and Systems, New York, pp. 93-98, May 17-19, 1978.

45. "Error Control Techniques for Array Processors," 1977 International Symposium on Information and Theory, Ithaca, New York, October 1977.

46. "Fault-Tolerant Fail-Safe Logic Networks," Proceedings on IEEE Compcon, (with S.M. Reddy), pp. 363-366, March 1977.

47. "On Undetectability of Bridging Faults," Proceedings of 1977 International Symposium on Fault-Tolerant Computing, Los Angeles, California, (with K.L. Kodandapani), June 1977.

48. "Further Results on M-RMC Forms," Proceedings of 1976 International Symposium on Multivalued Logic, Logan, Utah, pp. 88-93, (with K.L. Kodandapani), May 1976.

49. "A Graph Structual Approach to Data Management Systems," Proc. Ninth Hawaii International Conference on System Sciences, (with L.C. Chang), Western Periodicals, pp. 254-258, January 1976.

50. "Fault-Tolerant Asynchronous Networks Using (2,1)-Type Assignments," Digest of Fifth International Symposium on Fault-Tolerant Computing, Paris, France, June 1975.

51. "Construction on Error Correcting Codes with Run-Length Limited Properties," presented in 1974 International Symposium on Information and Theory, Notre Dame, Indiana.

52. "Synthesis of Arithmetic and Logic Processors by using Nonbinary Codes ," Digest of Papers, Fourth International Symposium on Fault-Tolerant Computing, IEEE Computer Society Publications, (with L.C. Chang), pp. 4-22 .

53. "A Multi-Valued Switching Algebra Based on Finite Field," Proc 1974 International Symposium on Multiple Valued Logic, IEEE Computer Society Publications, Vol. 3, pp. 95-113.

54. "On Fault-Diagnosis of Sequential Machines," Proc. VI Hawaii Conference on System Sciences, Western Periodicals, (with S.M. Reddy), Januray 1973.

55. "A Design Technique for Synthesis of Fault-Tolerant Adders," Digest of Papers of 1972 International Symposium on Fault-Tolerant Computing, IEEE Computer Society Publications, (with S.M. Reddy), pp. 20-25.

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